Nonuniform threshold voltage profile in a-Si:H thin film transistor stressed under both gate and drain biases

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In this paper we show that an a-Si:H thin film transistor (TFT) stressed with bias temperature stress (BTS) under both gate bias and drain bias produces a nonuniform threshold voltage profile which can be obtained from the quasi-Fermi potential profile and the threshold voltage ($V_t$) shift data of BTS under the gate bias only. The transfer and output characteristics calculated with this nonuniform $V_t$-profile agreed well with the measured data, where the calculation was performed using both the gradual-channel approximation and independently the AIM Spice simulation with its level-15 a-Si TFT model. It is shown that local threshold voltage is high at the source and decreases toward the drain. Due to the nonuniform $V_t$-profile in the channel, the drain current level is higher in the forward direction, where the source and drain electrodes are the same between measurement and BTS, than in the reverse direction, where source and drain electrodes are interchanged. The forward and reverse I-V characteristics are somewhat similar to those of metal-oxide-semiconductor field-effect transistors with nonuniform channel doping. © 2008 American Institute of Physics. [DOI: 10.1063/1.3033527]

I. INTRODUCTION

The a-Si:H thin film transistors are used in analog circuits either as an active load device or as a pixel amplifier. An example of such a use is the thin film transistor (TFT) backplane circuitry for an active-matrix (AM) organic light-emitting diode display. In the backplane circuitry, a select TFT in the scan line operates in linear mode while a pixel amplifier in the data line operates in saturation mode. In the analog applications, the a-Si:H TFT device is subjected to a prolonged bias stress due to a constant dc bias; in contrast, the switching application undergoes the bias stress in pulsed mode with a Rather short duty cycle (such as a 33 $\mu$s positive pulse and a long negative pulse with a 16.6 ms periodicity). The prolonged dc bias stress and the different device operating modes cause the bias stress effects in the analog circuits to be different from those in switching circuits. In switching circuits, such as an AM liquid crystal display (AMLCD), the instability in threshold voltage, mobility, on/off current ratio, and subthreshold swing is usually studied in terms of gate bias stress only. However, in a saturation-mode operation of the TFTs in analog circuits, the gate bias and drain bias voltages are comparable to each other and together they determine the device instability. Even in the AMLCD switching pixel circuits, the drain bias may be significant in determining the threshold voltage ($V_t$)-shift. A few publications addressed the effect of drain bias in bias temperature stress (BTS), mainly the threshold voltage shift.1-3

Karim et al.1 reported the drain-bias dependence of $V_t$-shift in inverted staggered bottom gate TFT under bias stress at $V_{gs}$=15 V and various $V_{ds}$ at room temperature. They modeled the $V_{ds}$-dependence of $V_t$-shift by assuming that the $V_t$-shift is proportional to the total gate charge during stress. Their model agreed approximately with their experimental data, correctly showing the maximum $V_t$-shift at $V_{ds} = 0$ V and the minimum when the stress is in saturation mode. A more recent paper by Shringarpure et al.2 reported different forward and reverse I-V characteristics after a saturation-mode bias stress at room temperature. The forward characteristic is where the source and drain electrodes are the same as in bias stress experiment; the reverse characteristic is where the source and drain electrodes are interchanged after the bias stress experiment. They argued that the TFT channel after a saturation-mode stress consisted of two regions: one before the pinch-off point, where the channel is populated with defect states, and the other between the pinch-off point and drain, where the channel is free of any stress-induced defects.3 They argued that in the forward measurement the channel includes the stressed region and thus that the device shows a higher threshold voltage and lower $I_{dsat}$. However, in the reverse I-V measurement, they argued that the channel covers the unaffected portion which causes a lower effective $V_t$ and thus a higher $I_{dsat}$. Their interpretation in Ref. 2 of channel condition after a saturation-mode stress is essentially identical to the more detailed model for I-V characteristics in a hot-carrier stressed metal-oxide-semiconductor field-effect transistor (MOSFET) device by Quader et al.4 The model used by Quader et al.4 provides an interesting insight into the device physics after stress. Briefly, Quader et al.4 modeled a hot-carrier stressed MOSFET as composed of two regions of channel: an undamaged region toward the source and the damaged region toward the drain by the hot-carrier injection. They assumed that the damaged region is populated by uniform interface states. The uniform

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interface traps are acceptorlike and thus negatively charged when occupied. In the reverse $I-V$ characteristics where the hot-carrier stressed region is near the source, the trap states are fully charged, providing a maximum and uniform negative interface charge in the damaged region. In the forward $I-V$ characteristics, the hot-carrier stressed region is near the drain and the number of charged trap states either stays constant or varies with $V_{ds}$ depending on the quasi-Fermi level, which either stays constant (at low $V_{th}$) or decreases with increasing $V_{ds}$; while the trap states are constant in number and distributed uniformly. Also, the authors considered the screening effect at a high $V_{th}$ in part of the damaged region due to velocity saturation of carriers, which is not important in the case of $\alpha$-Si:H TFT due to the low carrier mobility.

In this paper we analyzed measured data using a position-dependent threshold voltage shift. The nonuniform $V_T$-profile, induced by a BTS with both gate and drain biases ($V_{d}$-BTS), is obtained from the uniform $V_T$-shift data under BTS with a gate bias stress only and the quasi-Fermi potential profile along the channel during $V_{d}$-BTS. This approach assumes that the local threshold voltage shift is proportional to the local overdrive stress and is consistent with the defect pool model.\textsuperscript{5,6} With this nonuniform $V_T$-profile, we calculate the transfer and output characteristics in forward and reverse directions and compare them to the measured data.

A TFT channel with a continuously varying local threshold voltage is similar to the nonuniform channel of a MOSFET with a nonuniformly doped channel (NUDC). The NUDC is a way to suppress undesirable short-channel effects,\textsuperscript{7} such as $V_T$ rolloff or channel punch through. NUDC is also present in lateral double-diffused and vertical double-diffused power MOSFET devices in which the channel is formed by a lateral diffusion difference between the $n^+$ source doping and the high-voltage $p$-doping under the gate. For a MOSFET with NUDC, the linear-mode transfer characteristic (TC) ($I_{ds}$-$V_{gs}$) is not quite linear and makes it difficult to extract the $V_T$ unambiguously. The NUDC MOSFETs have a position-dependent local threshold voltage, $V_T(y)$, and may be viewed as an infinite number of MOSFETs, each with a $V_T(y)$ at channel position $y$ and a differential channel length $dy$. Victory et al.\textsuperscript{8} used the charge-sheet model (CSM) to analyze the nonuniform doping along the channel. They divided the channel into $N$ segments, each with a uniform doping, where the gradual-channel approximation (GCA) formulas for MOSFET with a uniform channel were used for each uniform segment for surface potential, body-effect coefficient, bulk Fermi level, and channel mobility while an averaged channel charge and an average gradient of quasi-Fermi potential were used to calculate the channel current, with the constancy of channel current imposed across different segments. A system of $3N-3$ nonlinear equations for $3N-3$ unknowns were solved with a boundary condition on quasi-Fermi potential: $V_{th}=V_{th}$ and $V_{th}=0$. They compared this numerical solution to the device simulator PISCES simulation result. $N=8$ showed a good agreement with the transconductance ($G_m$) data, but $N<8$ showed an increasingly poor agreement with the decreasing $N$ with respect to the PISCES data for a $L=5.5$ $\mu$m MOSFET.\textsuperscript{8} Wang\textsuperscript{9} also analyzed the $I-V$ and transconductance characteristics of MOSFETs with a nonuniform channel doping. Dividing the channel into $N$ grids, the local $V_T(y)$ at the grid point $y_i$ was calculated to reflect the local doping level. Also, the gate-bias-dependent local mobility, $\mu(y)$, was calculated at the grid point. Local surface potential was solved using the CSM as a function of gate bias, quasi-Fermi potential, and bulk bias; the channel charge density was obtained in terms of local doping level and surface potential; and the GCA yielded the drain current. A matrix equation was solved numerically. Wang\textsuperscript{9} discussed the effect of peak doping location on $I_{ds}$-$V_{gs}$ and $G_m$-$V_{gs}$ characteristics. Moving the peak doping position toward the drain, the $I_{ds}$-$V_{gs}$ moved toward a higher $V_{gs}$, indicating a higher $V_T$. $G_m$ was more peaked as the peak of the doping profile was closer to the source and smoother as the peak doping profile moved away from the source. For a step-function profile of $N_A$, $G_m$-$V_{gs}$ was more peaked when the high concentration was at source side and smoother when the high $N_A$ was at drain side.

Based on the above observations of various approaches to the hot-carrier-stressed MOSFETs and MOSFETs with NUCD, we use a simple approach of considering the local $V_T$ and local carrier mobility in the $I-V$ calculation. Moreover, the nonuniform $V_T$-profile, $V_T(y)$, in the $\alpha$-Si:H TFT sample after $V_d$-BTS, is obtained from the $V_T$-shift data of a uniformly stressed sample by BTS with gate bias stress only. After a saturation-mode stress or after $V_d$-BTS in general, the $\alpha$-Si:H TFT channel is characterized by $V_T(y)$ and $\mu(y)$.

II. EXPERIMENTS

The amorphous-Si:H TFT device used in this study had an inverted staggered structure with a Mo/Al gate metal layer on a glass substrate, followed by 400-nm-thick silicon nitride gate insulator, $\alpha$-Si:H semiconductor layer, and Mo source and drain contact metal under the surface protective layer.\textsuperscript{10} Bias stress was done on a hot chuck, capable of setting sample temperature between room temperature and 300 °C, which was mounted on a probe station. All stress experiments and the $I-V$ characteristic measurements were performed at 100 °C. We chose a 100 °C stress temperature which exceeds the average (about 50 °C) or even the upper-end (about 70 °C) operating temperature of the AMLCD backplane circuits under backlighting because a higher stress temperature accelerates the $V_T$-shift and thus can provide a worst-case $V_T$-shift estimate in the reliability testing. This is also useful for devices in a harsh operating environment such as automotive applications where the upper-end operating temperature can easily exceed 70 °C. The BTS under gate bias stress was performed at a stress gate bias, $V_{gs}$, ranging from 0 up to 20 V for 1500 s with both drain and source terminals connected to ground. The $V_d$-BTS experiments were performed for 1500 s at a constant gate bias of $V_{gs}$=20 V and a selected drain bias, usually $V_{ds}$=20 V, with the source terminal connected to ground.

After each BTS or $V_d$-BTS had been completed, the linear and saturation transfer characteristics ($I_{ds}$-$V_{gs}$) were immediately obtained, followed by an output characteristic ($I_{ds}$-$V_{ds}$), with the sample on a hot chuck maintained at 100 °C, spending minimal time for the $I-V$ scans in order to
minimize the complications from annealing (because the sample temperature is at 100 °C during the measurements) or extra bias stress (because the I-V scans apply dc biases to sample). Typical scan times were about 4 s for each $I_d$-$V_{gs}$ scan for $V_{gs}$ from −20 to 20 V, 5–8 s for saving the data file, and 6–9 s for the $I_d$-$V_{ds}$ scans for $V_{ds}$ from 0 to 30 V with $V_{gs}$ set at three different voltages. The I-V scans were done with a HP4145B semiconductor parameter analyzer. After each stress and I-V scan experiment, the entire wafer was annealed at 180 °C for 2 h in an oven, which recovered the original sample characteristics. For the $V_{ds}$-BTS-stressed samples, the I-V characteristics were obtained in both forward and reverse directions. The order of data acquisition of the forward and reverse characteristics slightly affected the result because the thermal annealing during the previous I-V scan affected the next I-V data. Both BTS and I-V scans were conducted inside an electromagnetic interference (EMI)-shielded dark box.

III. EXPERIMENTAL RESULTS AND MODEL CALCULATION

For a stress voltage lower than some critical value ($V_{gs} < V_{gs1}$), it is generally accepted that the threshold voltage instability arises mainly due to state creation in the channel region; for a higher stress voltage ($V_{gs} > V_{gs1}$), the $V_{t}$-shift is caused by charge trapping in the silicon nitride dielectric.11 The critical voltage, $V_{gs1}$, depends on the stoichiometry of silicon nitride dielectric and is greater than 80 V for a stochiometric silicon nitride.11 In this work we applied a stress voltage $V_{gs}$ of up to 20 V, which is low enough for state creation to be the dominant mechanism. We briefly describe the state creation process according to the defect pool model.12,13 A detailed understanding of this model is useful in modeling the nonuniform channel after $V_{ds}$-BTS: the weak Si–Si bonds or equivalently the band tail states break and form the Si dangling bonds. In order to break, the weak bond must be occupied by an electron and the broken bond is stabilized by a hydrogen atom which must diffuse to the weak bond site.5 The weak bonds comprise of the band tail states and the dangling bonds form the deep states; the deep states are negatively charged in a $n$-type $a$-Si, and more defects are charged than neutral defects are neutral in an intrinsic $a$-Si:H.14 Negatively charged defects in a $n$-channel device raise the threshold voltage. The rate of increase in the density of dangling bonds is proportional to the product among the density of weak bonds, the occupancy of band tail states (and thus the electron density in the channel), and the hydrogen diffusion coefficient.5 Therefore, at a given stress voltage, temperature, and total stress time, the threshold voltage shift is proportional to the charge density $Q_{str}$ of band tail electrons which depends on the stress bias. Furthermore, $Q_{str}$ is not uniform under $V_{ds}$-BTS. For example, at the beginning of stress (when the $a$-Si:H TFT has a uniform threshold voltage, $V_{th}$), the local electron charge density at a stress bias $V_{gs}$ is given by

$$Q_{str}(y) = C_g(V_{gs} - V_{th} - V_{str}(y)),$$

where $C_g$ is the gate capacitance, $V_{th}$ is the initial threshold voltage, and $V_{str}(y)$ is the quasi-Fermi potential profile induced by the drain bias $V_{ds}$. For example, under a saturation-mode $V_{ds}$-BTS, the quasi-Fermi potential $V_{str}(y)$, calculated under the GCA, takes on a squared-root form with the apex at the pinch-off point.15 $V_{str}(y)$ for a saturation-mode stress is obtained from

$$1 - \frac{V_{str}}{V_{th}} = \sqrt{1 - \frac{y}{L_1}},$$

where the constants $V_{th}$ and $L_1$ are found, for example, by the following: defining the pinch-off point ($y = L_1$) as the position where the electric field $dV_{str}/dy$ reaches an arbitrarily large value (e.g., $3 \times 10^8$ V/cm or near the dielectric breakdown field of Si); assuming that this constant electric field exists throughout the depletion region between the pinch-off point and drain, which satisfies the requirement of electric field continuity throughout the channel; and using the condition $V_{str}(L) = V_{ds}$ where $L$ is the channel length. Equation (2) gives the quasi-Fermi potential in channel between source and pinch-off point. Equation (2) was used to obtain the $V_{th}$-profile after $V_{ds}$-BTS and the $I-V$ curve in the gradual-channel approximation and was illustrated in Fig. 1(A). Equation (2) is similar to the channel potential in Ref. 15; however, in Ref. 15 the electric field $dV_{str}/dy$ becomes infinite at the pinch-off point while we assume a very large yet finite $dV_{str}/dy$ at the pinch-off point and in the depletion region.

Before the pinch-off point during a saturation-mode bias stress, the distribution of gate overdrive voltage along the channel is given by $V_{str}(y) = V_{gs} - V_{th} - V_{str}(y)$, which is illustrated in Fig. 1(A). This stress produces a nonuniform charge density as given by Eq. (1) and consequently a nonuniform
We neglected any effect of the local negative bias stress in channel is depleted and is under a negative overdrive stress. Coordinate along the channel. Beyond the pinch-off point, the local gate overdrive voltage is because the quasi-Fermi potential substantially reduces the length

Before and after the stress, a linear TC was measured at $V_{ds}$=20 V before and after saturation-mode extrapolation method depends on mobility only as $\sqrt{\mu_{FE}(V_{gs})}$ while the triode-mode extrapolation method depends on $\mu_{FE}(V_{gs})$ linearly.

A linear regression of the BTS data of $V_t$ versus $V_{gs}$ is as follows:

$$V_t = A + BV_{gs},$$

where $A$=-0.453 V and $B=0.288$ based on the saturation-TC-extracted $V_t$ data in Fig. 2. The nonuniform $V_t$-profile after a saturation-mode $V_{ds}$-BTS with $V_{gs}$=20 V and $V_{ds}$=20 V is

$$V_t(y) = A + B[V_{gs} - V_{sat}(y)],$$

where $V_{sat}(y)$ is found from Eq. (2). $V_t(y)$ is shown in Fig. 3. We use this $V_t$-profile and calculate the linear and saturation $I$-$V$ characteristics after the $V_t$-BTS at 100 °C for 1500 s, using the GCA and independently, using the AIM Spice simulation.

A. The GCA calculation

The nonuniform channel in a long-channel device is handled here in terms of a position-dependent threshold voltage and a position-dependent mobility in the gradual-channel approximation. Transistors with a nonuniform channel include $a$-$Si$:H TFTs after $V_{ds}$-BTS and MOSFETs with a nonuniform doping or after a hot-carrier stress,

$$I_d = WQ(y)\mu_{FE}(y)\frac{dV}{dy},$$

Q(y) = C_g[V_{gs} - V_t(y) - V(y)].
The extracted field-effect mobility was found to be approximately constant within about ±3%. Therefore, we assumed that the field-effect mobility has a negligible dependence on the stress voltage under the stress conditions here. After a V_{ds}-BTS, any channel position dependence of \( \mu_{\text{FE}} \) then comes from the position dependence of threshold voltage, \( V_t(y) \). For an \( \alpha \)-Si:H TFT with a uniform channel and threshold voltage \( V_{th} \), the field-effect mobility is modeled as

\[
\mu_{\text{FE}} = \frac{\mu_0}{V_{AA}^\gamma} (V_{gs} - V_{th})^\gamma,
\]

where \( \mu_0 \) is the band mobility with a default value of 10 cm²/V s and \( V_{AA} \) and \( \gamma \) are fitting parameters. After a 20 V BTS at 100 °C for 1500 s, we extracted the AIL Spice level-15 model parameters following the procedure in Ref. 16, which yielded \( V_{AA}=1.65 \times 10^8 \) V and \( \gamma=0.253 \). After V_{ds}-BTS, the local field-effect mobility of Eq. (7) is changed to

\[
\mu_{\text{FE}} = \frac{\mu_0}{V_{AA}^\gamma} [V_{gs} - V(y)]^\gamma.
\]

Integrating Eq. (5) with the field-effect mobility of Eq. (8), we obtain the following GCA formula:

\[
I_d = \frac{WC_G}{L} \int_0^{V_d} dV[V_{gs} - V(y) - V(y)] \mu_{\text{FE}}(y).
\]

Here, \( L' = L \) and \( V_{ds}' = V_{ds} \) for the triode-mode measurement and \( L' = L_{sat} \) and \( V_{ds}' = V_{ds} \) for the saturation-mode measurement, where \( L_{sat} \) is the distance between source and pinch-off point and \( V_{ds} \) is the quasi-Fermi potential at the pinch-off point. The quasi-Fermi potential during measurement, \( V(y) \), was obtained using Eq. (2) where \( V(y) \) replaces \( V_{sat}(y) \). Using the \( V_t \)-profile in Fig. 3, Eq. (9) was numerically integrated to obtain the linear-mode and saturation-mode transfer characteristics (\( I_d=V_{gs} \)) and the output characteristics (\( I_d=V_{ds} \)) for \( 3\times10^{-8} \) F/cm².

The calculated (solid lines) linear-mode and saturation-mode transfer curves are compared with the experimental data (symbols) in Figs. 4(A) and 4(B), respectively, for the forward (source and drain are the same as in stress) and reverse (source and drain are interchanged from stress) characteristics. For the linear-mode transfer curves, the forward and reverse characteristics were the same. The saturation-mode drain current \( I_d \) is higher in the forward direction than in the reverse direction. The reverse data taken right after the forward data with the sample maintained at 100 °C showed a small but significant thermal annealing effect. The time (4–5 s) required to complete a transfer curve measurement was enough to produce a small yet significant reduction in the \( V_t \)-shift due to thermal annealing. Therefore, we made two independent measurements, one measurement with forward first and reverse next and, after a 180 °C 2 h thermal annealing followed by an identical \( V_{ds} \)-BTS stress, the other measurement was made with reverse first and forward next. The two forward \( I-V \) data and the two reverse data were averaged, respectively, in order to cancel out any annealing-caused discrepancy between the forward and reverse data. The averaged forward and reverse \( I-V \) data are shown in Fig. 4. The good agreement between the GCA-calculated transfer and output characteristics with the experimental data indicates that the \( V_t \)-profile shown in Fig. 3 is indeed correct after the saturation-mode of 20 V \( V_{ds} \)-BTS at 100 °C for 1500 s. The good agreement also suggests that under our stressing conditions, the assumption that the field-effect mobility \( \mu_{\text{FE}} \) is independent of the stress voltage is reasonable.

The difference between forward and reverse saturation-mode TCs is mainly due to the \( V_t \)-profile (see Fig. 3) which is the highest at the source-end for forward and the highest at the drain-end for reverse. Elaborating on this, let us make a simplifying assumption that \( \mu_{\text{FE}} \) is constant throughout the channel. Then, Eq. (9) becomes

\[
I_d = \frac{W}{L'} \mu_{\text{FE}} C_g \frac{V_{gs} - \frac{1}{2} V_d V_d}{1 + J},
\]

where \( J \) is the channel average of the local threshold voltage normalized by the local overdrive voltage \( V_{ov}(y) \).
Figure 5 shows the channel average of a normalized local threshold voltage, \( V_{\text{gs}} \), as a function of the measurement gate bias, \( V_{\text{gs}} \), for forward and reverse measurements in linear and saturation modes, respectively. For the above-threshold region (e.g., \( V_{\text{gs}} \) greater than the maximum local \( V_t \)), the linear-mode characteristic has nearly the same \( V/V_{\text{ov}} \) in forward and reverse directions. However, the saturation mode has a \( V/V_{\text{ov}} \) which is clearly greater in the reverse direction than in the forward direction except for a low \( V_{\text{gs}} \) region (lower than about 6 V). Therefore, it may be concluded that the forward saturation current is higher than the reverse saturation current because of the lower average normalized threshold voltage. It is also interesting to note that, compared to the reverse case, the forward \( V_{\text{gs}}(V)/V_{\text{ov}}(y) \) is relatively flat along the channel, with only a slightly increasing tendency from the source (high-\( V_t \) region) toward the drain (low-\( V_t \) region). This is illustrated in Fig. 5(B) for \( V_{\text{gs}}=20 \) V and \( V_{\text{gs}}=20 \) V. This means that the channel affects the forward drain current almost uniformly. However, the profile of reverse \( V_{\text{gs}}(y)/V_{\text{ov}}(y) \) increases more rapidly from the source (low-\( V_t \)) toward the drain (high-\( V_t \)), with a pronounced increase near the drain end of channel (the highest-\( V_t \) region). Therefore, the reverse drain current is affected strongly by the drain side, particularly the highest-\( V_t \) region. It is also interesting to note that the difference in the forward and reverse transfer curves will lead to a different extracted threshold voltage if a simple extrapolation method is used on the measured data. The resulting discrepancy in extracted \( V_t \) will be further discussed later in this paper.

B. Circuit model and spice simulation

The nonuniform channel after \( V_{\text{dr}} \) BTS was divided into \( N \) segments where each segment had a channel length of \( L/N \) and a uniform threshold voltage corresponding to the average of local \( V_t \) values. The \( N \) series-connected TFTs had their body terminals merged together as Fig. 6 shows. The field-effect mobility parameters \( \mu_0, \gamma, \) and \( V_{\text{AA}} \) and all device parameters except for the threshold voltage were the same for all component TFTs. This “series-connected transistor” model is shown in Fig. 6. We used the AIM spice circuit simulator with the level-15 \( \alpha \)-Si:H TFT model to simulate the transfer and output characteristics. The above-threshold parameters of the level-15 model were first extracted for the experimental data of 20 V 1500 s BTS-stressed sample at 100 °C, following the procedure in Ref. 16. The extracted level-15 parameters that are different from the default values are shown in the table of Fig. 6. The device parameters including the \( V_t \) profile and field-effect mobility are the same as they were in the GCA calculation of Fig. 4. Figure 7 shows both simulated and experimental linear and saturation transfer characteristics and output characteristics. A very good fit between simulated and experimental data is obtained in all three \( V-I \) characteristics. This result supports the validity of the series-connected transistor model of Fig. 6 and reinforces the validity of the \( V_t \) profile shown in Fig. 2 and the validity of the procedure, that is, replacing the gate overdrive voltage, \( V_{\text{gs}}-V_0 \), in the \( \Delta V_t \) versus \( V_{\text{gs}} \) data of BTS by a local overdrive voltage, \( V_{\text{gs}}-V_0-V_{\text{ter}}(y) \), to obtain the \( V_t \) profile in a \( V_{\text{dr}} \)-BTS stressed sample. The local overdrive stress voltage used in obtaining the \( V_t \) profile is consistent with the defect pool model.
IV. DISCUSSION AND SUMMARY

We showed in this paper that the $V_t$-BTS with a nonzero drain bias produces a nonuniform threshold voltage profile in a-Si:H TFT. The nonuniform profile of $V_t$ was obtained from the $V_t$-shift versus $V_{gs}$ data of BTS by considering the quasi-Fermi potential profile during BTS. In the $V_d$-BTS stressed sample, the maximum local $V_t$ occurs at the source and the minimum occurs at the drain. The maximum $V_t$ at the source after $V_d$-BTS equals the $V_t$ value after a BTS with the same $V_{gs}$. The linear and saturation transfer characteristics, as well as the output characteristics, were calculated using the $V_t$-profile $V_t(y)$ shown in Fig. 2 based on the gradual-channel approximation. Good agreement was obtained as shown in Fig. 4. Furthermore, the graded $V_t$-profile was modeled as $N$ series-connected TFT devices with their body terminals merged, where each component TFT had a uniform channel and a channel length of $L/N$. Excellent agreement was obtained between the experimental data and the spice simulation for $N=10$. The agreement was still good for the model transistor components as few as $N=5$. The nonuniform local threshold voltage profile (higher at source and lower at drain) resulted in a forward drain current higher than the reverse current for saturation mode. The linear-mode transfer characteristics at $V_{ds}=0.1$ V were nearly the same in both forward and reverse directions.

The different forward and reverse saturation-mode transfer characteristics for the same sample with a nonuniform $V_t$-profile will lead to a different extracted $V_t$ value. In the extrapolation method, the threshold voltage is obtained by extrapolating the straight portion of the $I-V$ data in either the linear $I_d-V_{gs}$ plot for linear transfer curves or the $\sqrt{I_d-V_{gs}}$ plot for saturation transfer curves. The $V_{gs}$-intercept of this extrapolation is taken as the $V_t$ value. Figure 8 shows the extracted $V_t$ by extrapolation from both simulated and experimental transfer characteristics which were shown in Figs. 4 and 7 where the simulated data were based on the $V_t$-profile of Fig. 2. The extracted $V_t$ from the forward saturation-mode transfer curve is lower than that from the reverse curve by about $0.5 \pm 0.1$ V. This is mainly because the nonuniform $V_t$-profile affects the forward and the reverse curves differently through the different values of normalized $V_t$ (see Fig. 5). Figure 8 also shows that the extracted $V_t$'s from the linear transfer curves are higher than those from forward saturation-mode transfer curves by as much as $1.0 \pm 0.1$ V. This higher $V_t$ from the linear-mode data seems to be caused mainly by the influence of the $V_{gs}$-dependence of field-effect mobility on the transfer $I-V$ curve. The extracted $V_t$ from the saturation-mode transfer curve is much less sensitive to the field-effect mobility than the linear transfer $I-V$ because of a reduced $V_{gs}$-dependence (the power-law dependence is $\gamma$ for saturation versus $\gamma$ for linear) and due to a substantially reduced gate overdrive voltage caused by the high quasi-Fermi potential in the channel in a saturation-mode biasing. These reasons seem to be responsible, at least partially, for the observation that the extracted $V_t$ from the saturation-mode transfer curve is close to the AIM Spice level-15 model parameter $V_{th}$ as shown in Fig. 2.