Electrical measurements of voltage stressed $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSFET

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Abstract

Electrical characteristics of GaAs metal–oxide–semiconductor field effect transistor with atomic layer deposition deposited $\text{Al}_2\text{O}_3$ gate dielectric have been investigated. The $I$–$V$ characteristics were studied after various constant voltage stress (CVS) has been applied. A power law dependence of the gate leakage current ($I_g$) on the gate voltage ($V_g$) was found to fit the CVS data of the low positive $V_g$ range. The percolation model well explains the degradation of $I_g$ after a high positive $V_g$ stress. A positive threshold voltage ($V_{th}$) shift for both $+1.5$ V and $+2$ V CVS was observed. Our data indicated that positive mobile charges may be first removed from the $\text{Al}_2\text{O}_3$ layer during the initial CVS, while the trapping of electrons by existing traps in the $\text{Al}_2\text{O}_3$ layer is responsible for the $V_{th}$ shift during the subsequent CVS.

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1. Introduction

GaAs based field effect transistor (FET) has attracted much interest on high speed or high power applications due to its advantages over Si based FETs. The electron mobility of GaAs is five times larger than that of Si which leads to a faster logic operation. Its high breakdown voltage is useful for high power applications. In comparison to the conventional GaAs metal–semiconductor FET (MESFET), depletion mode GaAs metal–oxide–semiconductor FET (MOSFET) has some advantages. For example, GaAs MESFET has limitations in high leakage current and in the small forward gate bias required due to low Schottky barrier height. To realize a feasible GaAs MOSFET, extensive efforts have been made to find a high quality and thermally stable insulator on GaAs with a low interface trap density. Much progress has been made recently to form a high quality high-$k$ gate oxide on GaAs surface, such as e-beam evaporated $\text{Ga}_2\text{O}_3$ [1] and atomic layer deposition (ALD) grown $\text{Al}_2\text{O}_3$ [2].

The high-$k$ gate dielectrics have been extensively studied during the last decade. Promising results show potential replacement of $\text{SiO}_2$ with the high-$k$ gate dielectrics on a Si substrate in the CMOS technology [3,4]. In comparison to other high-$k$ gate dielectrics, $\text{Al}_2\text{O}_3$ has a large band gap (9 eV), a relatively high dielectric constant (8.6–10), a high breakdown field (5–10 MV/cm) and high thermal stability up to 1000 °C. Ye et al. [2] characterized the depletion mode $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSFET and found a very high drain current and a relatively high transconductance. The negligible drain current hysteresis [2] indicated that both the $\text{Al}_2\text{O}_3$ layer and the $\text{Al}_2\text{O}_3/\text{GaAs}$ interface are of a good quality.

The reliability study of $\text{Al}_2\text{O}_3$ gate dielectric in the depletion mode GaAs MOSFET has not been reported much in the literature. In this paper, we report the results of voltage stress effect of $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSFET using constant voltage stress (CVS). First, we report the data on the gate leakage current in the $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSFET before and after a high positive gate bias stress has been applied. Second, we report the threshold voltage ($V_{th}$) variation during the positive CVS. Power law dependence of the threshold voltage shift ($\Delta V_{th}$) with the stress time was confirmed.
2. Experimental

The depletion mode n-channel Al$_2$O$_3$/GaAs MOSFET was fabricated using a standard CMOS process. The device structure is shown in Fig. 1. The n-type Si-doped ($4 \times 10^{17}$/cm$^3$) GaAs layer was grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. An Al$_2$O$_3$ gate dielectric was deposited at a substrate temperature of 300°C using the atomic layer deposition (ALD) technique. The high-$k$ layer is as thin as 8 nm, which is equivalent to 3.1 nm of SiO$_2$ for the same capacitance value. The interface quality was further improved by a post-deposition annealing at 600°C for 60 s in an oxygen ambient. The source and drain Ohmic contacts were formed by e-beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 435°C anneal in a forming gas ambient. Finally, Ti/Au metals were e-beam evaporated to form the gate electrodes. The source-to-gate and the drain-to-gate spacings were 1 μm. The gate width is 100 μm and gate length is varied among the tested samples.

It is well known that a SiO$_2$ interfacial layer will be grown simultaneously when a high-$k$ gate dielectric is deposited on a Si substrate. This interfacial layer could be a passivation layer which lowers the interface trap density and improves the interface quality [3,4]. However, it contributes to the total gate oxide capacitance as a series capacitance along with the high-$k$ oxide capacitance. This decreases the total gate dielectric constant. For the GaAs MOSFET we studied, it was suggested that there may be a several angstroms thick Ga–oxide interfacial layer between Al$_2$O$_3$ and GaAs substrate [2]. Any possibility of SiO$_2$ layer between Al$_2$O$_3$ and GaAs substrate was not considered possible, because the doping concentration of Si impurities in GaAs was low. Frank et al. [5] reported that Ga(As) oxide layer grows spontaneously on the GaAs substrate during the ALD of Al$_2$O$_3$ and that only Ga$_2$O$_3$ interfacial layer remains after a thermal treatment at 600°C which decomposes the interfacial As–oxides and removes oxygen. Any effect of the Ga–oxide layer is discussed later in this paper.

CVS was applied to investigate the stress effects on GaAs MOSFET and the Al$_2$O$_3$ gate dielectric. Gate leakage current with increasing the stress time was monitored during CVS. $I-V$ characteristics including gate current ($I_g$) vs. gate voltage ($V_g$) and drain current ($I_{ds}$) vs. gate voltage ($V_g$) were measured using the HP-4145B parameter analyzer. Measurements were taken periodically to monitor the variation during CVS.

3. Results and discussion

The gate leakage current ($I_g$) of virgin samples with different gate areas is shown in Fig. 2. The gate voltage ($V_g$) sweep was done only between −3 V and 3 V. The virgin samples in Fig. 2 clearly show a very large asymmetry of $I_g$ under different polarities of $V_g$ sweep, in which the $I_g$...
at positive $V_g$ is about six to seven orders of magnitude higher than that at negative $V_g$. A possible reason is the different work function between the n-type GaAs substrate ($\sim$4.13 eV) and the gate electrode (Ti/Au, $\sim$4.75 eV) for which an average value of Ti (5.30 eV) [6] and Au (4.2 eV) [6] work functions was used. As was mentioned earlier, a very thin Ga$_2$O$_3$ layer may exist between Al$_2$O$_3$ and GaAs substrate. Ga$_2$O$_3$ has an energy band gap (2.45 eV) and a dielectric constant of $\sim$10, which is close to the Al$_2$O$_3$ dielectric constant of 8.6–10. Although, the potential barrier between Al$_2$O$_3$ and Ga$_2$O$_3$ is unknown, it is likely that Ga$_2$O$_3$ layer does not affect the carrier injection for both of the gate voltage polarities, because it has a small band gap energy compared to Al$_2$O$_3$ (9 eV). The barrier height of Ti–Au/Al$_2$O$_3$ is much larger than that of Al$_2$O$_3$/GaAs so that the electrons will require more energy to overcome the barrier to be injected through the gate oxide under a negative $V_g$ sweep than in the positive $V_g$ sweep. The asymmetry of gate current density was also observed in the studies of high-$k$/SiO$_2$ stack on a Si substrate [7]. Although, the SiO$_2$ interfacial layer which exists in the high-$k$/Si system plays an important role in the carrier injection through the high-$k$ gate dielectric, the Ga$_2$O$_3$ interfacial layer does not seem to play a role in the carrier injection in this Al$_2$O$_3$/GaAs system.

It is also possible that a depletion layer in n-type GaAs that formed in the negative gate voltage, and no such depletion in the positive gate voltage, could cause the asymmetry of $I_g$ in the unstressed virgin samples. In other words, the asymmetry in gate leakage current will arise, because the $n$-type GaAs surface will be in accumulation for positive gate voltage and in depletion for a negative gate voltage. The voltage drop across the depletion layer will account for the asymmetry. A rough estimation indicates that the surface potential, $\Psi_s$, can be three times as large as $V_{ox}$, the oxide voltage drop, when GaAs surface is in depletion. On the other hand, when $V_g$ is positive and the GaAs surface is in accumulation, most of $V_g$ will drop across the gate oxide. Here, $\Psi_s$ and $V_{ox}$ are related by

$$V_g = V_{fb} + \Psi_s + V_{ox}$$  \hspace{1cm} (1)

where $V_{fb}$ is the flat band voltage. The $V_{fb}$ in this depletion mode MOSFET was roughly estimated using the gate bias where the transconductance, $g_m$, is maximum [2]. The $V_{fb}$ estimated from the $g_m$ data is about 0.37 V for the virgin device and the oxide charge, $Q_{ox}$, is as high as 1.56 x $10^{12}$ q/cm$^2$ using the following equation:

$$V_{fb} = \varphi_{ms} - \frac{Q_{ox}}{C_{ox}}$$  \hspace{1cm} (2)

where $\varphi_{ms}$ is the work function difference between the gate electrode Ti/Au and the GaAs substrate, which is approximately 0.62 V and $C_{ox}$ is the oxide capacitance of 9.956 x $10^{-7}$ F/cm$^2$.

Fig. 3 shows $I_g$-$V_g$ characteristics for a $40 \times 100$ $\mu$m$^2$ GaAs MOSFET with +6 V CVS with the increasing stress time. It shows that for $V_g$ between 0 V and 0.35 V, the gate leakage current increases by two to three orders of magnitude after a long time CVS. For $V_g$ greater than 0.35 V, the $I$-$V$ characteristics of the stressed sample before breakdown are similar to the virgin sample. This indicates that there may be two different mechanisms involved in the degradation of gate leakage current by the high positive $V_g$ stress. Houssa et al. [8,9] explained the soft breakdown of ultrathin SiO$_2$ gate oxides using the percolation theory of nonlinear conductor networks. They reported that when the soft breakdown occurs, the current behaves according to a power law dependence on the applied gate voltage. Fig. 4 shows $V_g$-$I_g$ characteristics after the stress and before the breakdown on a log–log scale. The data behaves according to a power law:

$$V_g = \rho_{eff} I_g^x$$  \hspace{1cm} (3)
where $\rho_{\text{eff}}$ is the effective resistivity of gate oxide, and $a = 0.90 \pm 0.03$ as shown in Fig. 4. $\rho_{\text{eff}}$ extracted from Fig. 4 clearly decreases as the stress time is increased.

The power law dependence of $V_{\text{g}}$–$I_{\text{g}}$ characteristics suggests that the percolation model plays a role in the degradation process of the gate leakage current under the positive high gate bias stress. The percolation model as proposed by Degraeve et al. [10] is detailed in the following. As the positive high gate bias is applied, a large number of traps (or broken bonds) are generated within the gate dielectric layer and at the interface. We assume that these traps randomly occupy the sites within the oxide. When a critical number of traps are generated, they will form a percolation path between the gate and the substrate, leading to a sudden increase in the gate current. With the breakdown, the paths become a permanent conductive filament and current flows directly between the gate and the substrate. This model explains that after breakdown, the leakage currents show an Ohmic behavior for both polarities. Fig. 3 shows that after the breakdown, $I_{\text{g}}$ increased about six orders of magnitude over that of the virgin device. Similar data from positive CVS on HfO$_2$/Si sample by Chatterjee et al. [11] showed a dramatic increase in the leakage current after the hard breakdown.

In Fig. 3, when $V_{\text{g}}$ sweep is greater than 0.35 V, the gate leakage currents are similar before or after the CVS. Houssa et al. [9] claimed that this is caused by Fowler–Nordheim tunneling. However our extracted barrier height from the data according to the Fowler–Nordheim tunneling model was unreasonably large. A good fit of $I_{\text{g}}$ vs. $V_{\text{g}}$ for $V_{\text{g}}$ greater than 0.35 V was obtained with $I_{\text{g}} = a e^{bV_{\text{g}}}$. This does not correspond to any conduction model that we know.

$I_{\text{ds}}$ vs. $V_{\text{g}}$ characteristics are measured to verify the threshold voltage ($V_{\text{th}}$) reliability under positive CVS. The $V_{\text{th}}$ is extracted from $I_{\text{ds}}$ vs. $V_{\text{g}}$ data by a linear extrapolation. The $V_{\text{th}}$ shift ($\Delta V_{\text{th}}$) is defined as the difference between the stressed sample and the virgin sample. Fig. 5 shows $\Delta V_{\text{th}}$ at various stress voltages at room temperature, 20°C. Virgin samples with an area of 20 $\mu$m x 100 $\mu$m are used in each measured curves. $I_{\text{ds}}$ vs. $V_{\text{g}}$ at $V_{\text{ds}}$ = 0.1 V was measured immediately after each positive CVS, within about 2 s of the CVS. It is observed that $V_{\text{th}}$ shifts positive at the beginning of the stress cycle and becomes saturated with the increasing stress time for both +1.5 V and +2 V CVS (Fig. 5). Both $\Delta V_{\text{th}}$ curves have similar shapes but increase with the increasing stress voltage. The positive $V_{\text{th}}$ shift indicated that a significant number of electrons were getting trapped in the high-$k$ gate dielectric during the positive CVS. Gate leakage current density ($J_{\text{g}}$) and the subthreshold slope with increasing the stress time were also measured for both +1.5 V and 2 V CVS. Fig. 6 shows the power law dependence of $J_{\text{g}}$ on the stress time. $J_{\text{g}}$ decreased very slightly and continuously with prolonging the stress time. This implied that there is no trap created in the bulk of Al$_2$O$_3$ gate dielectric during the positive CVS. Fig. 7 shows the dependence of the subthreshold
the Al\textsubscript{2}O\textsubscript{3} so that the trapped electrons will increase the value, as shown in Fig. 5. Once the mobile charges are removed from the oxide, any further \( V_{\text{th}} \) shift will be caused by the electrons trapping in Al\textsubscript{2}O\textsubscript{3}. To reinforce this argument, we performed negative CVS experiments on some samples (Fig. 8). Same \( I_{\text{ds}} \) vs. \( V_{\text{g}} \) measurements were applied after each negative CVS. After the negative CVS, some \( V_{\text{th}} \) shift was again positive after the initial negative CVS, similar to the positive CVS data. A removal of positive mobile charges, but not the injection and trapping of holes, can explain this small positive shift of \( V_{\text{th}} \) under the negative CVS. After this initial period, Fig. 8 shows that \( V_{\text{th}} \) shifts negatively upon further stress time as expected from the injection and trapping of holes in the high-\( k \) gate dielectric.

It is useful to mention that the \( I_{\text{ds}} \) vs. \( V_{\text{g}} \) measurements were conducted within a few tenths of volts below and above the \( V_{\text{th}} \) with a negative \( V_{\text{g}} \) sweep range (−0.8 V to −0.2 V). We were concerned that the negative \( V_{\text{g}} \) sweep used in the \( V_{\text{th}} \) measurement could cause some de-trapping, because of its opposite stress polarity from the positive CVS, even though the \( I_{\text{ds}} - V_{\text{g}} \) measurement will last only for about 0.4 s. From a control experiment, we estimate an approximate \( V_{\text{th}} \) shift of 2.46 mV caused by an \( I_{\text{ds}} \) vs. \( V_{\text{g}} \) measurement which is conducted between positive CVS steps. This \( \Delta V_{\text{th}} \) is negligibly small compared with the \( V_{\text{th}} \) shift caused by the positive CVS.

4. Summary

In this work, we investigated the leakage current through the Al\textsubscript{2}O\textsubscript{3} gate dielectric in a depletion mode GaAs MOSFET after a various constant voltage stress had been applied. The observed asymmetry of leakage current in virgin device was discussed in relation to the work function difference between gate electrode and GaAs substrate. The leakage current after the stress was discussed in terms of the percolation model. The positive \( V_{\text{th}} \) shift observed for both +1.5 V and +2 V CVS indicated an electron trapping in the Al\textsubscript{2}O\textsubscript{3} gate dielectric by the existing traps. The continuously decreasing gate leakage current density and the constant threshold voltage slope with the increasing

\[
\Delta V_{\text{th}} = \Delta V_{\text{max}} (1 - \exp(-t/\tau_0))
\]

where \( \Delta V_{\text{max}} \) is the maximum threshold voltage shift, \( t \) is the stress time, \( \tau_0 \) and \( \beta \) are fitting parameters. \( \tau_0 \) is related to the capture cross-section \( \sigma_0 \) as \( \tau_0 = \frac{4}{\beta \sigma_0} \) (\( \sigma_0 \) is the initial gate leakage current density as shown in Fig. 6). This model is based on the assumption that the traps have continuously distributed capture cross-section [12]. Fig. 5 shows the calculated result (solid lines) and the experimental data (symbols) for various stress conditions. The calculated results agreed well with the experimental data when the stress time is greater than about 10 s. The fitting parameter \( \beta \) is 0.34, which is consistent with the result on Al\textsubscript{2}O\textsubscript{3} by Zafar et al. [12]. Other parameters \( \Delta V_{\text{max}} \) and \( \tau_0 \) depended on the stressing voltages. The model of \( \Delta V_{\text{th}} \) vs. stress time, as expressed by Eq. (4), works well except for about first 10 s of stressing. From Eq. (4) and Fig. 5 it can be seen that \( \Delta V_{\text{th}} \) would become saturated with prolonging the stress time further.

The positive shift of \( V_{\text{th}} \) at the beginning of the stress cycle may also arise if any positive mobile charges that may exist in the high-\( k \) gate dielectric of the virgin sample are removed during the initial stages of stress time. As was mentioned earlier, the oxide charge is high, about \( 1.56 \times 10^{12} \) q/cm\textsuperscript{2}. It is possible that once the positive \( V_{\text{g}} \) is applied, the positive mobile charges are quickly repelled from the high-\( k \) gate dielectric to the GaAs substrate. This may explain the significant overshoot of the experimental data point within the first 10 s of stress over the calculated value, as shown in Fig. 5. Once the mobile charges are removed from the oxide, any further \( V_{\text{th}} \) shift will be caused by the electrons trapping in Al\textsubscript{2}O\textsubscript{3}. To reinforce this
stress time implied that no new traps are created during the +1.5 V and +2 V CVS. Power law model of $\Delta V_{th}$ vs the stress time by Zafar et al. was found to fit our experimental data well. Our data analyses implied that during the initial 10 s period of CVS, mobile positive charges may be removed from the Al$_2$O$_3$ layer, and during the subsequent CVS, the trapping of carriers injected into Al$_2$O$_3$ is responsible for the $V_{th}$ shift.

References


