A comparison of ionizing radiation and high field stress effects in $n$-channel power vertical double-diffused metal-oxide-semiconductor field-effect transistors

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$n$-channel power vertical double-diffused metal-oxide-semiconductor field-effect-transistor (VDMOSFET) devices were subjected to a high electric field stress or to x-ray radiation. The current-voltage and capacitance-voltage measurements show that the channel-side interface and the drain-side interface are affected differently in the case of high electric field stress, whereas the interfaces are nearly uniformly affected in the case of x-ray radiation. This paper also shows that for the gated diode structure of VDMOSFET, the direct-current current-voltage technique measures only the drain-side interface; the subthreshold current-voltage technique measures only the channel-side interface; and the capacitance-voltage technique measures both interfaces simultaneously and clearly distinguishes the two interfaces. The capacitance-voltage technique is suggested to be a good quantitative method to examine both interface regions by a single measurement. © 2005 American Institute of Physics.

[I. INTRODUCTION]

When a metal-oxide-semiconductor (MOS) device is exposed to a high electrical field stress, electrons are injected into the gate oxide from Si bulk via Fowler-Nordheim (FN) tunneling. A fraction of the injected electrons creates additional electron-hole pairs in the oxide through impact ionization.1–3 The generated electron-hole pairs result in oxide-trapped charges or in interface traps. This is similar to the effects of ionizing radiation in MOS devices.4

Recently, several authors have reported results from high field stress test studies of vertical double-diffused power metal-oxide-semiconductor field-effect-transistors (VDMOSFETs).5–8 Schwalke et al. used the high field stress test as an accelerated reliability testing method for the gate oxide.5 Others used the test result from a high field stress test as a screening method for devices which are to be operated in a radiation environment.6–8 In particular, Picard et al. suggested that the high field stress test could be used as a device selection technique for the radiation environment without an actual radiation test.6 They found similarities in their isochronal annealing results in the charge trapping characteristics between the ionizing radiation and the high field FN injection. Stojadinovic et al. reported experimental results and theoretical models of oxide-charge trapping and interface trap generation under a high field stress condition.7,8

Some earlier studies also compared the results of high field stress effects with ionizing radiation effects.9–12 Boesch and McGarrity proposed that the high field stress measurements may be used to predict the total dose radiation hardness.9 Electrical measurements have shown that the generation of interface traps is proportional to the concentration of oxide-trapped holes.10,11 However, an electron spin resonance study showed that a trivalent silicon hole trap, termed an $E'$ center, did not account for most of the positive charges generated by a high field stress, whereas it accounted for most of the positive charges in the irradiated oxides.12

Since a VDMOSFET has two different parts of interfaces under the gate oxide, one interface in the MOSFET channel region and one interface at the drain surface (see Fig. 1), experimental studies indicated that the two interfaces behaved differently under an ionizing radiation.13–15 Moreover, comparing the results from different experimental techniques was difficult in VDMOSFET.13–15 Picard et al.6 and Stojadinovic et al.7,8 used the subthreshold current-voltage technique16 and the single transistor mobility technique17 in their studies. These techniques produce information only on the channel-side interface.

In this paper, we report results from a high field stress study and an x-ray irradiation study. Our results clearly show that the areal distribution of oxide-trapped charges and inter-

FIG. 1. A simplified cross-section view of a half cell VDMOSFET with high frequency capacitance-voltage measurement setup and its internal capacitance components.
face traps is not uniform along the gate oxide/semiconductor interface when the sample has been subjected a high field stress, where as the trap distribution is approximately uniform in x-ray irradiated samples. We studied the drain-side interface by the direct-current current-voltage (DCIV) technique and the channel-side interface by the subthreshold midgap IV (MG) technique, respectively. A high frequency capacitance-voltage (CV) technique was used to examine both interfaces in a single measurement. The data obtained from the CV technique are compared with the data obtained using the DCIV and subthreshold IV techniques.

Our results further show that investigating the total ionizing dose effects or the high electric field stress effects in both parts of the interface region can improve on the understanding of the device degradation process during the device operation in normal or radiation environment. We show that the CV technique is a very simple and effective tool for monitoring the degradation of the gate oxide in both interface regions, simultaneously. It also enables us to examine both interface regions quantitatively.

II. EXPERIMENTAL DETAILS

We used two IRF510 (TO-220AB) n-channel power VDMOSFET samples manufactured by Fairchild Semiconductor, Inc., rated at 5.6 A and 100 V. It had a nominal gate oxide thickness of 100 nm and channel length of 1.0 μm.

One sample was irradiated with x ray from a Cu-target x-ray generator with 45 kV and 10 mA setting. The x-ray dose rate was calibrated using another IRF510 VDMOSFET sample by irradiating it with a calibrated 137 Cs γ-ray source and was estimated to be 23.6 rds/s (SiO₂). During the irradiation, all three terminals of the device were grounded. The irradiation was performed at 5 min steps and after each step we measured the IV and CV data. Total accumulated dose was 35.4 krds after five irradiation steps. The CV, DCIV, and subthreshold IV data were taken after 5 min had elapsed at the end of each irradiation step.

For the high field stress experiment a constant voltage of +70 V was applied to the gate of a virgin VDMOSFET device. The source and drain terminals were connected to the ground. The gate voltage corresponded to an electric field of \(E ≈ 7\) MV/cm in the gate oxide layer. During the stress, we monitored the gate current \(I_G\). The gate stress was interrupted at various times during the stress to perform the designated experiments. CV, DCIV, and subthreshold IV data were promptly taken, and then the stress was resumed. The three techniques used in this study could probe different regions of the oxide-silicon interface as mentioned earlier.

Figure 1 illustrates a half cell VDMOSFET cross section along with its internal capacitance components. Based on the subthreshold IV technique, \(I_D-V_G\) characteristics were measured with a 100 mV drain to source bias applied. The DCIV data were obtained with a forward bias of 0.3 V applied to the \(pn\)-junction between the \(p\)-type body and the \(n\)-type drain. For the DCIV data, the current was measured between source and drain while the gate voltage was scanned. Figure 1 also shows the CV experimental setup for the capacitance measurement between gate and source \((C_{GS})\). A 1 MHz, 15 mV (rms) sinusoidal ac signal was superimposed on a dc bias voltage from an external power supply while the drain terminal was connected to the ground. This arrangement makes the drain terminal a floating terminal for the ac test signal. All experiments were performed at room temperature.

III. RESULTS AND DISCUSSION

Figure 2 shows the data obtained from an x-ray irradiated n-channel power VDMOSFET. The current peak in the DCIV data of Fig. 2(a) corresponds to a surface recombination current due to interface traps under the drain-side oxide. The current peak increases and shifts to a negative gate voltage direction as the accumulated dose increases. The
difference in the peak voltage positions between two data
reflects a net difference in \( Q_{ot} + Q_{it} \) near the midgap voltage of
the drain-side interface, where \( Q_{ot} \) is the positive oxide
charge and \( Q_{it} \) is the interface trap charge. The increase in
the current peak \( \Delta I_{peak} \) was previously shown to be propor-
tional to the increase in the interface trap density \( \Delta N_{it} \). Figure
2(b) shows the subthreshold \( I_d - V_{gs} \) characteristics after
irradiation. The voltage shift at the threshold current \( I_{th} \)
represents the sum of the shifts due to oxide-trapped charge
and interface-trap charge, i.e., \( \Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \). \( \Delta V_{it} \)
shift at the midgap current \( I_{mg} \) is the shift caused by the
changes in the oxide-trapped charge, i.e., \( \Delta V_{mg} = \Delta V_{ot} \). This
is the consequence of an assumption that the net interface-
trap charge is neutral when the Fermi level is at the
midgap. \( 16 \)

Figure 2(c) is the gate capacitance \( C_{GS} \) data after the
irradiation. The overall \( C_{GS} - V_{GS} \) curve is seen to shift to the
negative voltage direction as the dose increases. However,
the voltage variations in the two sides of the CV curves are
not equal. Interface traps cause the CV data to stretch out
along the gate voltage axis as interface-trap occupancy
changes with the gate voltage and oxide-trapped charges
cause the overall CV data to shift along the gate voltage axis
with respect to ideal CV data. \( 20 \) In addition, the CV data
obtained between the gate and source terminals consist of
capacitance components from drain side \( (C_{oxd} \text{ and } C_{sd}) \),
channel side \( (C_{oxb} \text{ and } C_{sb}) \), insulator \( (C_{im}) \), and other para-
metics as illustrated in Fig. 1. Contribution of these capaci-
tance components to the measured capacitance depends on
the surface potential at a given gate voltage. We can analyze
the CV data by separating it into the two regions, drain-side
interface and channel-side interface, because part of the CV
data that results from the surface potential variation in a
given region does not affect the surface potential variation
in other interface parts of the sample. For example, the capacitance of the left-hand side in the CV data is from
the \( n \)-type drain-side interface, while the step rise on the
right-hand side of the curve is from the channel-side inter-
face. A detailed analysis and modeling of the high frequency
CV data in a VDMOSFET will be published elsewhere. \( 21 \)

Comparison of the CV data before and after irradiation
provides us with information on the changing densities of
oxide-trapped charges and interface traps. Extracting the ca-
citance value at the midgap voltage \( V_{mg} \) or at the flat-band
voltage \( V_{fb} \) is not very useful due to the complexity of ca-
pacitance data at those voltages. \( 21 \) In contrast, the capacitance
value at the threshold voltage \( V_{th} \) for either of the two interfaces
[\( V_{th-drain} \text{ for the drain side and at } V_{th-ch} \text{ for the
channel side in Fig. 2(c) }] \) is almost free from interference by
the other interface. Consequently, the threshold voltage variation \( \Delta V_{th} \) in the \( C_{GS} \) data solely reflects the variations in
\( Q_{ot} + Q_{it} \) at that interface only. Thus, the variation in
the threshold voltage can simply be written as

\[
\Delta V_{th} = \frac{\Delta Q_{th}}{C_{th}} = \frac{\Delta Q_{ot} + \Delta Q_{it}}{C_{th}} = \Delta V_{ot} + \Delta V_{it}, \tag{1}
\]

where \( C_{th} \) is the capacitance at the threshold voltage and is
assumed to be constant.

In Fig. 2(c), \( V_{th,ch} \) was obtained by the subthresh-
old IV method. The capacitance at \( V_{th,ch} \) was denoted as
\( C_{th,ch} \). The figure was found by extrapolating the
lower knee on the left-hand side of the \( C_{GS} \) curve to the gate
voltage axis. The capacitance at \( V_{th-drain} \) is denoted as
\( C_{th,drain} \). Note that \( V_{th-drain} \) is close to the threshold voltage
of the drain-side MOS capacitor. The actual threshold voltage
is about \( V_{GS} = -1.2 \) V for the drain-side capacitor. Extract-
ing \( V_{th-drain} \) by extrapolation does not include much error.

The voltage shift after irradiation, i.e., \( \Delta V_{th-drain} \)
and \( \Delta V_{th,ch} \) at \( C_{th,drain} \) and \( C_{th,ch} \), reflect the net change in
\( Q_{ot} + Q_{it} \) at the drain-side and channel-side interfaces,
respectively.

The voltage shift as a function of the irradiation time,
based on the data in Fig. 2(a) through Fig. 2(c), is shown in
Fig. 2(d). As can be seen in the figure, the voltage shift at the
channel-side interface is about 30% larger than that at the
drain-side interface after the maximum irradiation dose. This
shows that the yield of positive oxide charge is different at
the two interfaces. The oxide charge trapping depends
greatly on the internal electric field inside the gate oxide
layer in ionizing radiation. \( 3 \) This difference in the yield of
oxide charge due to different internal electric field exists
whenever an external voltage bias is applied. \( 14 \) Figure 2(d)
demonstrates a good agreement in the voltage shift data between
CV and DCIV for the drain-side interface and between CV
and subthreshold IV for the channel-side interface. Fur-
thermore, this agreement among the three different techniques
also exists in the high field stress results.

A high field stress to the gate causes an oxide-trapped
charge generation and an interface-trap buildup. \( 6 \) Figure 3
shows data on a voltage-stressed device measured by the
DCIV and MG techniques. We also measured the time evolu-
tion of the gate current \( I_G \) during the voltage stress. Figure
3(e) shows that during the stress, the positive gate current \( I_G \)
increased rapidly until it reached a maximum value \( I_{G,max} \).
After \( I_{G,max} \), the gate current decreased gradually upon fur-
ther stress.

Figure 3(a) shows that the DCIV current peak increases
gradually and the voltage position of the current peak shifts
to the negative direction initially, as the stress time increases.
In Fig. 3(a), the curve marked as \( " + I_{G,max} \) corresponds to
the stress duration of a maximum gate current of Fig. 3(e). With a further stress time beyond \( I_{G,max} \), the current peak
increases but the position of current peak shifts to the posi-
tive voltage direction. The MG data in Fig. 3(b) show a
different response. The shifts in the threshold voltage and
in the midgap voltage show that the oxide-trapped charge
generation is still the dominant process, not the interface-trap
buildup, even after \( I_{G,max} \). A further stress duration produces
a large interface-trap buildup at the channel-side interface
while the oxide-trapped charges increase steadily.

In Fig. 3(c), the \( C_{GS} \) vs voltage curve shifts and stretches
out in the negative voltage direction until the gate current
reaches its maximum values \( I_{G,max} \) in the \( I_G \) vs stress time
data [see Fig. 3(e)]. However, the incremental voltage shift
takes the positive direction after \( I_{G,max} \). This indicates
the fact that after \( I_{G,max} \), there is a net negative charge gen-
eration from the interface-trap buildup at the interface and
or a decreased net positive charge, leads to a decreased elec-
consistent with the fact that an incremental negative charge,
the electron trapping in the gate oxide. This result is also
the electron trapping in the gate oxide. This result is also
consistent with the fact that an incremental negative charge,
or a decreased net positive charge, leads to a decreased elec-
tron tunneling current due to the increased barrier width in
Fowler-Nordheim tunneling. Schwalke et al.\textsuperscript{5} and Picard et al.\textsuperscript{6} also explained the evolution of the gate current by a
charge trapping kinetics in the oxide layer so that the gate
current increases by hole trapping and decreases by electron
trapping. Stojadinovic et al.\textsuperscript{7} argued that the decrease in
the gate current after the maximum $I_{G_{\text{max}}}$ is due to the interface
trap buildup, which can compensate for the local electric
field. As Fig. 3(d) shows, the stress responses of the two
interface regions are significantly different. In the channel-
side interface, while the gate current increases, the increasing
voltage shift indicates an increasing oxide charge. During a
later stress period, data indicates that the voltage shift by the
oxide-trapped charges is fully compensated by the increasing
negative charge, which is likely from the interface-trap
buildup\textsuperscript{5,6} and the electron trapping in the gate oxide.\textsuperscript{5,6} Since
the net charge state of the interface traps is positive at the
threshold voltage of drain side, the interface traps will make
the threshold voltage shift further to the negative voltage.
The data shown in Figs. 3(a) and 3(d) indicate a significant
amount of electron trapping in the drain-side gate oxide,
which overcomes the interface trap buildup beyond $I_{G_{\text{max}}}$.

Figure 3 shows that the threshold voltage variation in the
drain-side interface region is more prominent than the varia-
tion in the channel-side interface region. The threshold volt-
age shift in the drain-side interface reached a maximum at
$I_{G_{\text{max}}}$ while that in the channel-side interface continued fur-
ther as the stress time increased. This indicates that the oxide
charge trapping and the interface-trap buildup are different in
the two interfaces. This observation is in contrast with the
models discussed in Refs. 5–7, which may be appropriate for
one of the interfaces, but not for both interfaces. Moreover,
the modeling was done only for the channel-side interface
region.\textsuperscript{6,7} Also, localization of the stress-induced oxide
charges and interface traps in the drain-side MOS capacitor
can be caused by a nonuniform electric field distribution. A
small change in the electric field intensity in the gate oxide
can cause a large change in the gate current, which governs
all processes in the oxide charge trapping and the interface-
trap buildup.\textsuperscript{6}

Figure 4 shows another difference in the effects pro-
duced by an ionizing radiation and the effects produced by a
high field stress. In the figure, the diode saturation current,
$I_{\text{sat}}$, and the ideality factor $n$ are plotted as a function of stress
or irradiation time. The data were reduced from the DCIV
data obtained at various $pn$-junction biases $V_{pn}$.\textsuperscript{14,15} In our pre-
vious studies of x-ray and y-ray irradiated samples,
changes in the peak current $\Delta I_{\text{peak}} = (I_{\text{peak}} - I_{\text{sat}})$ and the back-
ground bottom current $I_{\text{sat}}$ were found to be directly propor-
tional to the accumulated dose. $\Delta I_{\text{peak}}$ was dependent on the

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**FIG. 3.** High field stress responses on an $n$-channel power VDMOSFET (IRF510). (a) DCIV data; (b) subthreshold IV data; (c) interterminal capacitance voltage, $C_{DC}$; (d) voltage shift data extracted from (a) through (c); and (e) evolution of the gate current $I_G$ during the stress corresponding to the stress voltage $V_G=70$ V. The source and drain terminals were shorted and grounded. The broken lines in (c) indicate the data for stress time after $I_{G_{\text{max}}}$ in (e).
gate bias and $I_{\text{bot}}$ was independent of the gate bias applied during irradiation. However, for the high field stressed sample, the results are different from the irradiated sample. As can be seen in Fig. 4(b), the $\Delta I_{\text{peak}}$ saturation current behaved similarly to the irradiated sample during the stress time and the $\Delta I_{\text{peak}}$ ideality factor showed a different evolution in the stress time periods before and after $I_{G_{\text{max}}}$. Since the positive oxide-trapped charge generation is the dominant process in the stress time period before $I_{G_{\text{max}}}$, $I_{\text{peak}}$ will change significantly in voltage position but not in its magnitude. After $I_{G_{\text{max}}}$ as the stress time increased, the ideality factor increased similarly to the irradiated sample and this is consistent with the fact that interface-trap buildup is the dominant process, leading to an increase in $\Delta I_{\text{peak}}$.

A more significant difference was observed in the variation of $I_{\text{bot}}$ in the DCIV data. As shown in Fig. 4, during the high field stress, the values of $I_{\text{sat}}$ and $n$ of $I_{\text{bot}}$ remained near their prestress values, while these values increased in the irradiated sample as the irradiation time increased. $I_{\text{bot}}$ is considered to be the forward-biased diode current without influence from the surface recombination under the gate oxide of the device and the increased $I_{\text{bot}}$ was easily annealed out at 100 °C. The origin of $I_{\text{bot}}$ variation is still not clear at this point. However, we can rule out the possibility of a radiation-induced recombination in the Si bulk or in the depletion region of the body-drain $pn$-junction because the incident photon energy is not high enough to create displacement damages in the Si bulk. If a high field stress is used to simulate the ionizing radiation, the increase in $I_{\text{bot}}$ cannot be simulated and the effects of this increased background leakage current may not be predicted.

**IV. SUMMARY**

Experimental data obtained from an $n$-channel power VDMOSFET after exposure to x-ray irradiation or to a high field stress were analyzed comparatively. The irradiation affected both the drain-side and channel-side interfaces, almost equally. However, the high field stress produced the oxide-trapped charge and the interface-trap buildup more concentrated on the drain-side interface. This is believed to be due to a stronger electric field in the drain-side interface than in the channel-side interface during the high field stress.

High field stress on the gate oxide did not increase the leakage current term $I_{\text{bot}}$ in the DCIV data, while the x-ray irradiated device showed a significantly increased $I_{\text{bot}}$. Simulating the ionizing radiation effects using a high field stress must consider these differences. It is suggested that both the drain-side interface and the channel-side interface should be examined separately for a correct interpretation of the ionizing radiation and the high field stress effects.

We analyzed both interface regions of an $n$-channel power VDMOSFET using the CV measurement. For the drain-side interface, the CV data were consistent with the DCIV data. For the channel-side interface, the CV data were consistent with the subthreshold IV data. Therefore, the CV measurement is shown to be a simple way to examine both interface regions under the gate oxide in a single measurement. The conventional techniques, such as charge pumping, subthreshold IV, and DCIV techniques, can examine only part of the interface regions of the VDMOSFET. Additional work may be necessary because the CV measurement only produced information for the net charge variation in both of the SiO$_2$/Si interfaces.

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