Designing resonant tunneling structures for increased peak current density

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We report a simple method to increase the peak current density in a double-barrier resonant tunneling structure by using a small band-gap emitter spacer layer. We have fabricated AlAs/GaAs/AlAs resonant tunneling structures using a $Ga_{1-x}In_xAs$ spacer layer in the emitter. The peak current density was increased systematically with the increasing indium content by a factor ranging from 2.5 at $x = 0.05$ to 5 at $x = 0.2$ from the value at $x = 0$. The increased peak current density was accompanied by increases in the peak voltage and peak-to-valley ratio. The lowering of the bottom of electron energy distribution in the GaInAs emitter spacer layer is shown to explain both the peak current and voltage increases. In the sequential tunneling picture, the peak current increases because of the increase in the number of resonant electrons which occurs if the bottom of energy distribution is lowered. We also report for the first time a strong bistability in the current-voltage characteristics at $T \leqslant 175$ K in the asymmetric spacer layer structure (GaInAs emitter, GaAs collector) in an otherwise symmetric structure.

Since the pioneering work of Esaki, Tsu, and Chang,[1] much experimental and theoretical work has been done on the double-barrier resonant tunneling structures (DBRTS). Studies have been done to clarify the structural parameters important for the static current-voltage (I-V) characteristics and the dynamical transport properties. Studies of the static I-V characteristics were largely aimed at improving the peak current density (J_p) and its peak-to-valley ratio (PVR). Significant improvements were acheived in the J_p and PVR values at 300 and 77 K by using strained pseudomorphic layers as the barrier,[5] well,[2-5] and spacer[2] layers, in such samples as AlAs/GaInAs/AlAs DBRTS on a GaAs substrate[2-4] and AlAs/InAs/AlAs DBRTS on an InP substrate.[5] These strained DBRTS samples were symmetric in their layer structure, making it difficult to clarify the role of each strained layer in the device characteristics, and thereby hindering the development of a simple design principle. We report here on the clear role of a GaInAs spacer layer, used in either an emitter region or a collector region in an otherwise symmetric AlAs/GaAs/AlAs DBRTS.

The structure was grown on an n^+ GaAs substrate by molecular beam epitaxy in the following order: (i) 0.5 μm of [Si] = 1×10^{18} cm^{-3} GaAs buffer, (ii) 50 Å of undoped GaAs spacer, (iii) 30 Å of undoped AlAs barrier, (iv) 50 Å of undoped GaAs well, (v) 30 Å of undoped AlAs barrier, (vi) 50 Å of undoped $Ga_{1-x}In_xAs$ spacer, and (vii) 0.5 μm of [Si] = 1×10^{18} cm^{-3} GaAs cladding layer. In order to study the dependence of the device characteristics on the composition of the GaInAs spacer layer, samples with five different x values (0, 5%, 10%, 15%, and 20%) were grown with all other growth parameters kept the same. Ohmic contacts were formed by evaporating AuGe alloys and annealing at 420 °C for 30 s in a rapid thermal furnace. Device sizes between 28×28 and 36×36 μm^2 were defined by the photolithography technique and wet chemical etch. The I-V curves of the diodes were obtained by a HP4145B Semiconductor Parameter Analyzer.

Figure 1 shows the conduction-band diagram under the peak forward bias at which the GaInAs spacer is in the emitter side. Under Luryi's sequential tunneling picture,[6] the peak current flows when the number of resonant electrons in the emitter is maximum, which occurs when the quasi-stationary resonance level (E_r) in the GaAs quantum well is aligned with the bottom (E_0 or E_x) of the electron energy distribution in the emitter spacer region. At 0 K, the number of resonant electrons equals $4\pi Am^*(E_f - E_r)/h^2$, where A is the diode area, m^* is the electron effective mass, E_f is the Fermi level in the emitter region, and h is the Planck constant. Therefore, the resonant tunneling current at a given bias is proportional to $E_f - E_r$, and the peak current density to $E_f - E_x$. Due to the substantially large experimental valley current density (J_v), we use a modified peak current density (J_p').

$$J_p'(x) = J_p(x) - J_v(x) = B(E_f - E_x), \tag{1}$$

where B is a proportional constant. The peak current density can be increased if E_x, the minimum electron energy in the emitter spacer region, can be lowered. When the emitter spacer layer is changed from GaAs to GaInAs, an additional bias voltage is required for the current peak.

$$V_p(x) - V_p(0) \approx (E_0 - E_x)(2b + w + s + sc)/q(b + 0.5w), \tag{2}$$

where $V_p(x)$ is the peak voltage as a function of x in $Ga_{1-x}In_xAs$, b is the barrier width, w is the well width, s is the spacer width, sc is the space-charge layer thickness due to the collector depletion, and q is the electron charge.

Figure 2 shows the I-V characteristics at 300 and 77 K. At 300 K, the negative differential resistance (NDR) is clearly observed under the forward bias with the peak current density increasing with the increase in the indium content in the emitter spacer GaInAs layer. However, the

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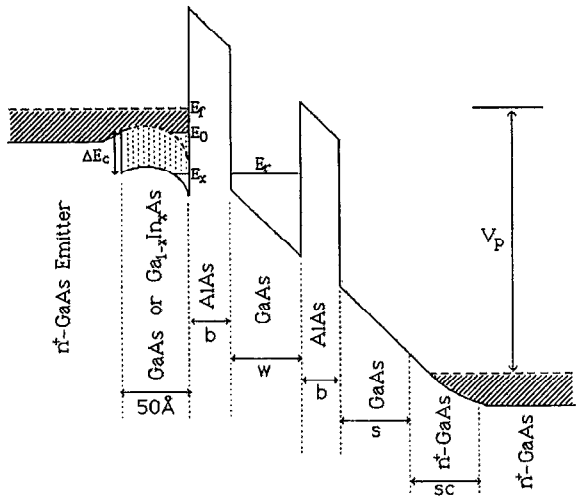
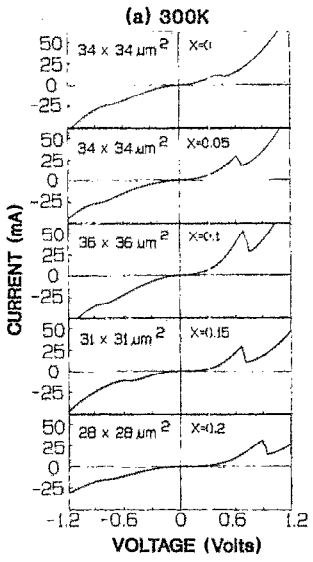


FIG. 1. Band diagram (not to scale) at peak forward bias V_p of the sample structures with $b = 30$ Å, $w = 50$ Å, and $s = 50$ Å. Note that the lowest electron energy in the emitter spacer region is lowered from E_0 in a GaAs spacer layer to E_x in a $Ga_{1-x}In_xAs$ spacer layer.



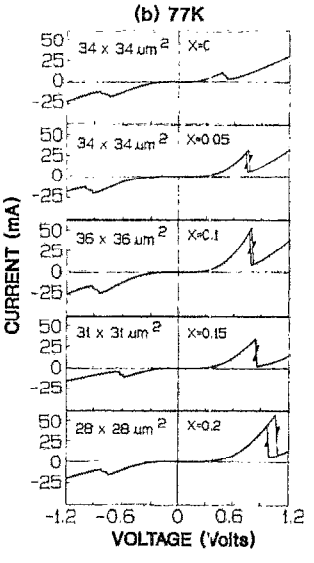


FIG. 2. I-V curves at (a) 300 and at (b) 77 K for samples with a $Ga_{1-x}In_xAs$ emitter spacer layer with $x = 0$, 5%, 10%, 15%, or 20%. Note the bistability at 77 K under the forward bias.

reverse bias NDR does not change appreciably with the changing indium content in the collector spacer GaInAs layer. Therefore, our data clearly demonstate that a lower band-gap GaInAs layer as an emitter spacer layer greatly improves the peak current density, while as a collector spacer layer it has little effect. The peak current density, peak-to-valley ratio, and the peak voltage at 300 and 77 K are listed in Table I, and all show a systematic increase with the increasing indium content in the emitter spacer, with some deviation of the $x = 15\%$ sample from the systematic trend. The reverse peak voltage of this $x = 15\%$ sample is somewhat smaller than the rest of the samples, suggesting a wider GaAs quantum well in this sample than in other samples. An x-ray interference analysis[7] using the conventional x-ray rocking curve technique showed that the thickness times composition product for the GaInAs layer in the $x = 15\%$ sample deviated from the nominal growth parameters by about 13% whereas the same product for other samples agreed with the nominal values almost exactly.

As Table I shows, the peak current density J_p increases from the value for $x = 0$ by a factor ranging from 2.5 for $x = 5\%$ to 5 for $x = 20\%$. V_p and PVR also increase systematically with the increasing x (with the already mentioned exception for $x = 15\%$). Even though these J_p, V_p, and PVR values are substantially improved over the AlAs/GaAs/AlAs symmetric DBRTS sample, a more important objective of this letter is to clarify the underlying physical mechanism and to establish a design method as represented by Eqs. (1) and (2) and Fig. 1. We show that the Eqs. (1) and (2) are satisfied (at least approximately) by our data. Equation (1) shows that $J_p'(x)/J_p'(0)$ should equal $(E_f - E_x)/(E_f - E_0)$. As listed in the eighth and ninth columns of Table I, the experimental data show a reasonable agreement with the estimated $(E_f - E_x)/(E_f - E_0)$ values. Here, we have assumed that $E_f - E_0 \approx 30$ meV, $E_0 - E_x \approx \Delta E_c$, and $\Delta E_c \approx 38$, 75, 113, or 150 meV for an indium content of 5%, 10%, 15%, or 20%, respectively. Assuming that $sc \approx 50$ Å, we estimate the $V_p(x) - V_p(0)$ values using Eq. (2), and the experimental and calculated values are listed in the tenth and last columns of Table I. Considering the possible errors in the structural parameters and diode sizes and the experimental variations in the peak voltage (± 0.05 V) and in the peak current density (± 0.25 kA/cm^2) among various diodes, comparison of the estimates with the experimental data shows an acceptable agreement. Also, the experimental data show that $[J_p'(x) - J_p'(0)]/[V_p(x) - V_p(0)]$ is about 5.0, 7.9, 8.6, and 6.9 for the indium contents of 5%, 10%, 15%, and 20%, respectively. This is roughly in consistency with the Eqs. (1) and (2) which indicate that this ratio should be constant, independent of x. We, therefore, conclude that the use of GaInAs material in the emitter spacer layer

TABLE I. Forward (positive) and reverse (negative) I-V data at 300 and 77 K. The ninth and last columns were estimated from $E_f - E_0 = 30$ meV and $E_f - E_x = E_f - E_0 + \Delta E_c$, $sc = 50$ Å, and Eqs. (1) and (2). The eighth and tenth columns are from the data at 77 K.

	300 K			77 K						
x in $Ga_{1-x}In_xAs$	V_p (V)	J_p (kA/cm^2)	PVR	V_p (V)	J_p (kA/cm^2)	PVR	$J_p'(x)/J_p'(0)$ *expt.*	$\frac{(E_f - E_x)}{(E_f - E_0)}$	$[V_p(x) - V_p(0)]$ expt.	calc.
0	0.36	1.01	1.12	0.47	0.95	3.61	1	1	0	0
	−0.71	−1.95	···	−0.74	−1.45	1.45	···	···	···	···
5%	0.62	2.42	1.64	0.73	2.4	4.95	2.8	2.3	0.26	0.15
	···	···	···	0.76	2.7	4.69	···	···	···	···
	−0.85	−2.22	···	−0.92	−1.67	1.55	···	···	···	···
10%	0.7	4.1	1.87	0.77	3.71	5.94	4.5	3.5	0.30	0.28
	···	···	···	0.8	4.03	5.86	···	···	···	···
	−0.79	−2.42	···	−0.85	−1.88	1.57	···	···	···	···
15%	0.66	2.86	2.69	0.84	3.42	13.7	4.6	4.8	0.37	0.43
	···	···	···	0.83	3.42	14.3	···	···	···	···
	−0.54	−1.23	1.02	−0.58	−1.03	2.67	···	···	···	···
20%	0.86	5.25	2.4	0.98	4.7	8.30	6.0	6.0	0.51	0.57
	···	···	···	1.05	5.12	7.31	···	···	···	···
	−0.71	−2.21	···	−0.76	−1.71	1.60	···	···	···	···

lowers the bottom of electron energy distribution in the emitter spacer region by approximately the conduction-band offset, increasing the number of resonant electrons for tunneling at the peak voltage.

We also have observed a strong bistability in the I-V data at 77 K of forward-biased RTD's with the GaInAs emitter spacer layer, as can be seen in Fig. 2(b). This bistability persisted up to the temperature of 175 K for $x = 0.2$ diodes, and above this temperature, the I-V characteristics showed a normal NDR behavior, as Fig. 2(a) shows. Addition of an external capacitor (ranging from 1 nF to 500 μF) in parallel with the DBRTS did not remove this bistability. The bistability in our data is similar in its characteristics to the intrinsic bistability of asymmetric barrier DBRTS which have been claimed by several workers.[8-10] Because of the increased peak voltage required in our diodes with a GaInAs emitter spacer layer, the collector barrier may become more transparent than the emitter barrier to the tunneling electrons, and therefore the asymmetric spacer (GaInAs emitter, GaAs collector) and symmetric barrier design seems to work against the intrinsic bistability mechanism. However, the much increased number of resonant electrons at the peak voltage could lead to a corresponding increase in the maximum electron storage by the GaAs quantum well, which will enhance the intrinsic bistability. An asymmetric spacer (with a lower gap emitter spacer) and asymmetric barrier (with a thicker or higher collector barrier) design could further enhance the intrinsic bistability. This phenomenon is under further investigation.

In conclusion, our I-V data for AlAs/GaAs/AlAs DBRTS with a GaInAs emitter spacer layer show that the use of a lower band-gap emitter spacer layer can lead to an increased peak current density and increased peak voltage. This is due to the lowered bottom of electron energy distribution in the emitter spacer region and hence the increased number of resonant electrons in Luryi's sequential tunneling picture. Our result is found to be consistent with the recent report on the tunneling from the quantized levels in the accumulation layer.[11] We also report the first observation of a strong bistability in the I-V data of DBRTS with an asymmetric spacer layer structure.

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